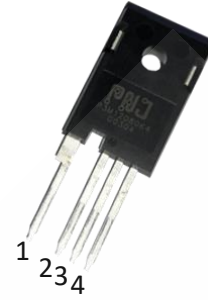




P3M12080K4 SiC MOS N-Channel Enhancement Mode

V_{RRM}	= 1200	V
I_D	= 47	A
$I_D (100^\circ\text{C})$	= 33	A
$R_{DS(on)}$	= 80	m Ω

SiC MOS P3M12080K4 N-Channel Enhancement Mode



Features

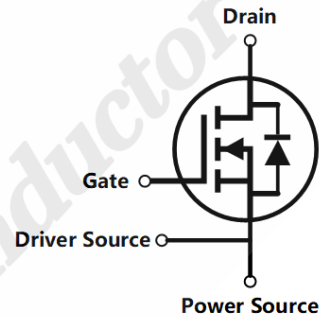
- Qualified to AEC-Q101
- High Blocking Voltage with Low On-Resistance
- High-Frequency Operation
- Ultra-Small Q_{gd}
- 100% UIS tested

Standards Benefits

- Improve System Efficiency
- Increase Power Density
- Reduce Heat Sink Requirements
- Reduction of System Cost

Application

- Solar Inverters
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies



TO-247-4

Drain	1
Source	2
Driver Source	3
Gate	4



Order Information

Part number	Package	Marking
P3M12080K4	TO-247-4	P3M12080K4



Contents

Features	1
Standards Benefits	1
Application	1
Order Information.....	1
Contents	2
1. Maximum Ratings	3
2. Electrical Characteristics.....	4
3. Reverse Diode Characteristics.....	5
4. Thermal Characteristics	6
5. Typical Performance	6
6. Package Outlines.....	11

PN Junction Semiconductor



1. Maximum Ratings

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	V_{DSmax}	1200	V	$V_{GS} = -3\text{V}$ $I_D = 100\mu\text{A}$
Gate - Source Voltage (dynamic)	V_{GSmax}	-8 / +19	V	AC ($f > 1\text{Hz}$)
Gate - Source Voltage (static)	V_{GSop}	-3 / +15	V	Static
Continuous Drain Current	I_D	47	A	$V_{GS} = 15\text{V}$ $T_C = 25^\circ\text{C}$
		33		$V_{GS} = 15\text{V}$ $T_C = 100^\circ\text{C}$
Power Dissipation	P_D	221	W	
Operating Junction	T_J	-55 To +175	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 To +175	$^\circ\text{C}$	
Solder Temperature	T_L	260	$^\circ\text{C}$	
Mounting Torque	M_d	1 8.8	Nm lbf-in	M3 or 6-32 screw



2. Electrical Characteristics

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	/	/	V	$V_{GS} = -3V$ $I_D = 100\mu A$
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.2	/	V	$V_{DS} = V_{GS}$ $I_D = 30mA$
		/	1.45	/	V	$V_{DS} = V_{GS}$ $I_D = 30mA$ $T_J = 175^\circ\text{C}$
Drain Current	I_{DSS}	/	0.14	10	μA	$V_{GS} = -3V$ $V_{DS} = 1200V$
Gate-Source Leakage Current	I_{GSS}	/	20	250	nA	$V_{GS} = 15V$ $V_{DS} = 0V$
Drain-Source On-State Resistance	$R_{DS(on)}$	/	80	96	m Ω	$V_{GS} = 15V$ $I_D = 20A$
Transconductance	g_{fs}	/	10.65	/	S	$V_{DS} = 20V$ $I_{DS} = 20A$
		/	11.5	/	S	$V_{DS} = 20V$ $I_{DS} = 20A$ $T_J = 175^\circ\text{C}$
Input Capacitance	C_{iss}	/	2070	/	pF	$V_{GS} = 0V$ $V_{DS} = 800V$ $f = 1MHz$ $V_{AC} = 25mV$
Output Capacitance	C_{oss}	/	78	/	pF	
Reverse Transfer Capacitance	C_{rss}	/	8	/	pF	
Coss Stored Energy	E_{oss}	/	53.1	/	μJ	
Turn-on Energy	E_{on}	/	243.8	/	μJ	$V_{DS} = 800V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Turn-off Energy	E_{off}	/	32.62	/		



P3M12080K4 SiC MOS N-Channel Enhancement Mode

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Turn-On Delay Time	$t_{d(on)}$	/	14.08	/	ns	$V_{DS} = 800V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Rise Time	t_r	/	15.68	/		
Turn-Off Delay Time	$t_{d(off)}$	/	23.2	/		
Fall Time	t_f	/	16.64	/		
Internal Gate Resistance	$R_{G(int)}$	/	1.76	/	Ω	$f = 1MHz$ $V_{AC} = 25mV$
Gate to Source Charge	Q_{gs}	/	20.8	/	nC	$V_{DS} = 800V$ $I_{DS} = 20A$ $V_{GS} = -3 \text{ to } 15V$ $I_G = 20mA$
Gate to Drain Charge	Q_{gd}	/	13.5	/		
Total Gate Charge	Q_g	/	57.2	/		

3. Reverse Diode Characteristics

At $T_J = 25^\circ C$, unless specified otherwise

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Diode Forward Voltage	V_{SD}	4.8	/	V	$V_{GS} = -3V$ $I_{SD} = 10A$
		4.6	/	V	$V_{GS} = -3V$ $I_{SD} = 10A$ $T_J = 175^\circ C$
Continuous Diode Forward Current	I_S	32	/	A	$V_{GS} = -3V$
Reverse Recover Time	t_{rr}	17.6	/	ns	$V_{GS} = -3V$ $I_{SD} = 20A$ $V_R = 800V$ $dI_f/dt = 5200A/\mu s$ $T_J = 25^\circ C$
Reverse Recovery Charge	Q_{rr}	610.33	/	nC	
Peak Reverse Recovery Current	I_{rrm}	53.62	/	A	

4. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.68	$^{\circ}\text{C}/\text{W}$

5. Typical Performance

At $T_J = 25^{\circ}\text{C}$, unless specified otherwise

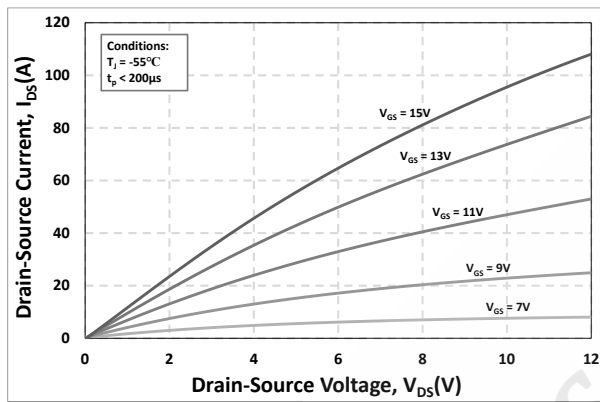


Figure 1. Output Characteristics $T_J = -55^{\circ}\text{C}$

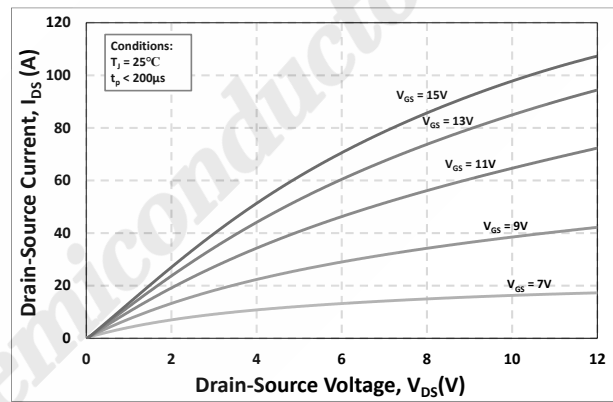


Figure 2. Output Characteristics $T_J = 25^{\circ}\text{C}$

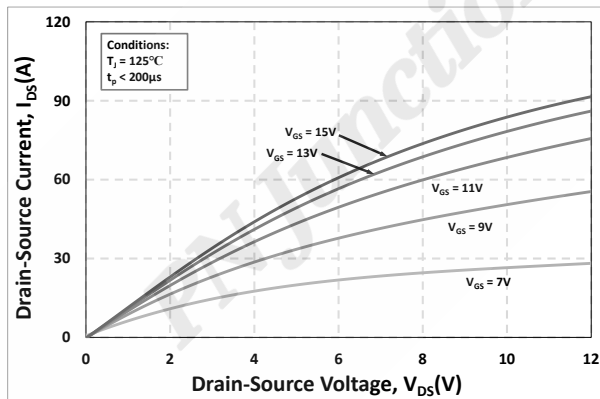


Figure 3. Output Characteristics $T_J = 125^{\circ}\text{C}$

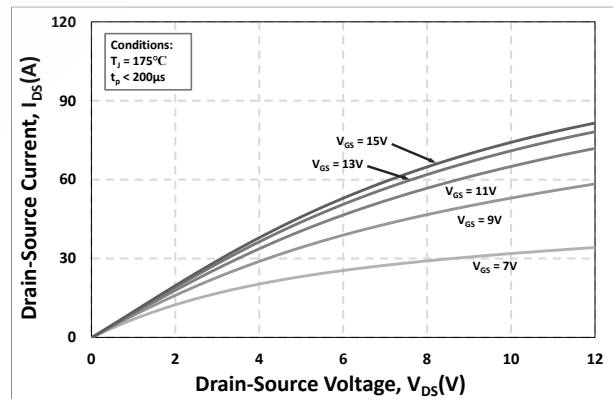


Figure 4. Output Characteristics $T_J = 175^{\circ}\text{C}$

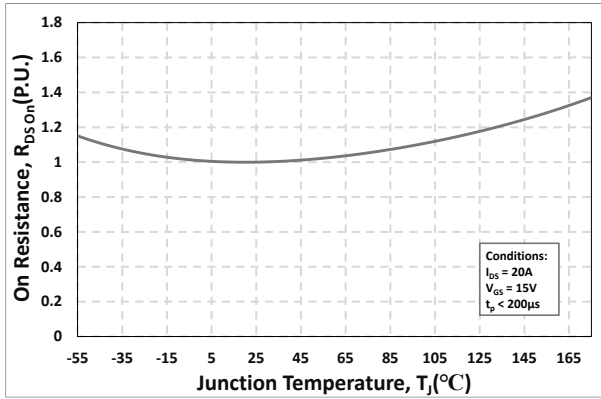


Figure 5. Normalized On-Resistance vs. Temperature

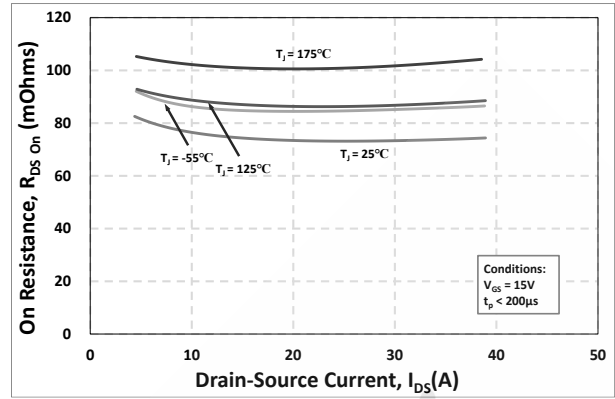


Figure 6. On-Resistance vs. Drain Current Various Temperatures

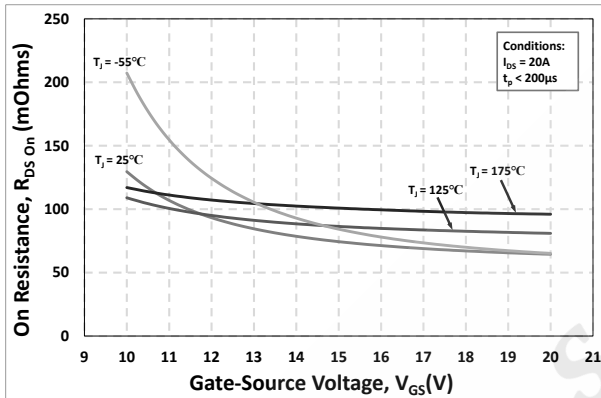


Figure 7. On-Resistance vs. Gate-Source Voltage

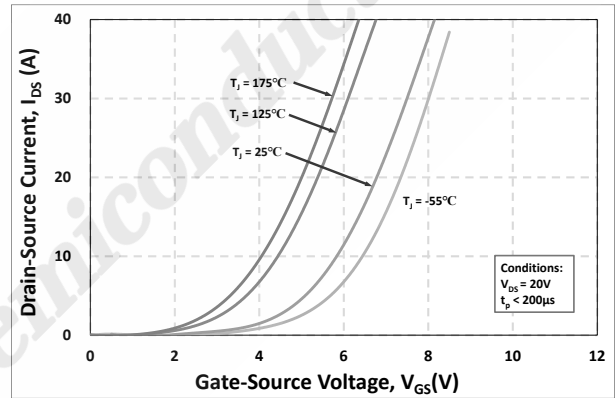


Figure 8. Transfer Characteristic for Various Junction Temperatures

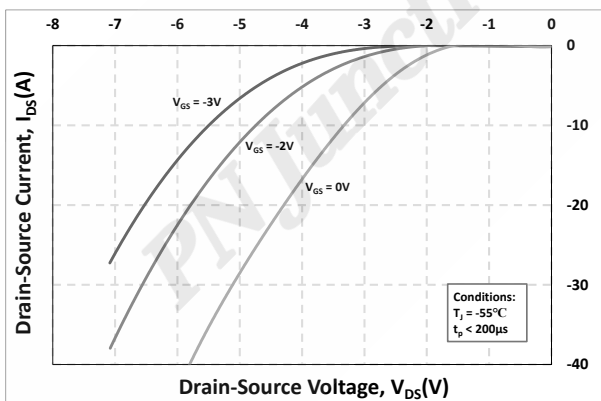


Figure 9. Body Diode Characteristic at -55°C

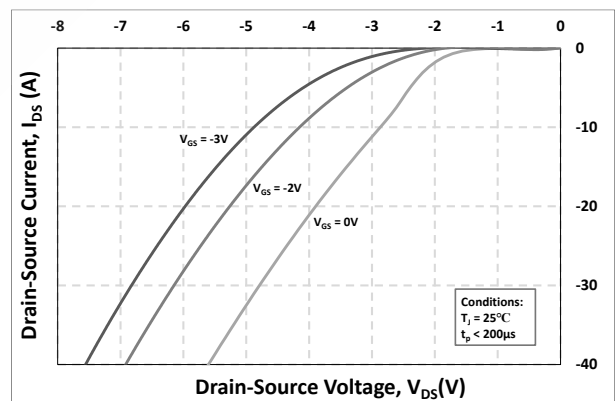


Figure 10. Body Diode Characteristic at 25°C

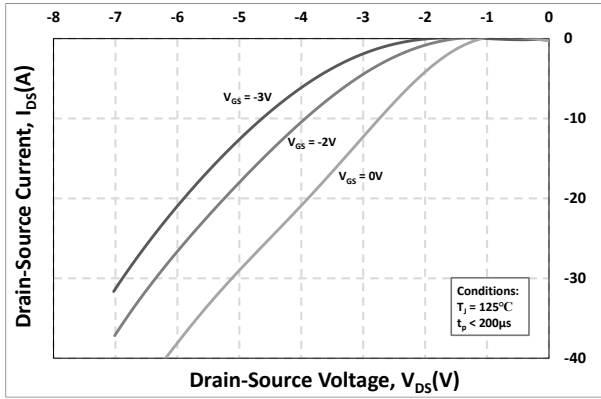


Figure 11. Body Diode Characteristic at 125°C

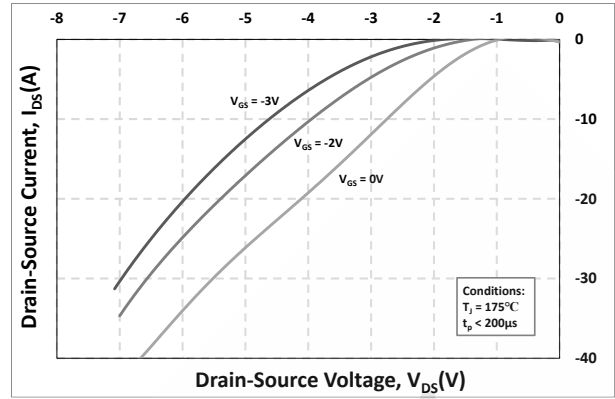


Figure 12. Body Diode Characteristic at 175°C

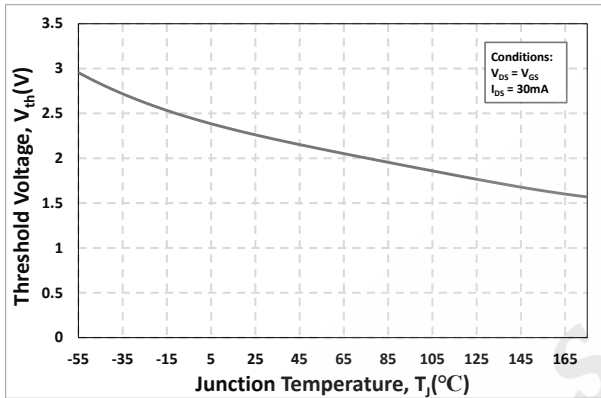


Figure 13. Threshold Voltage vs. Temperature

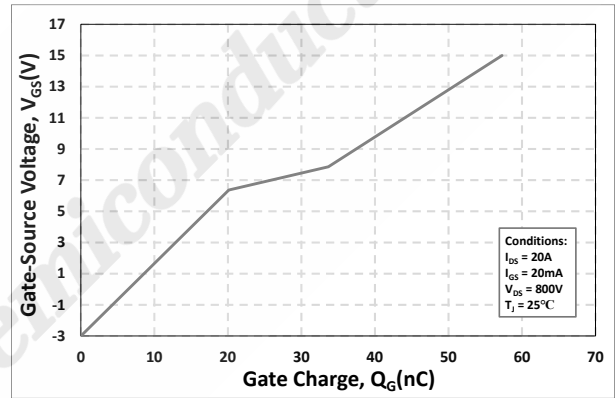


Figure 14. Gate Charge Characteristics

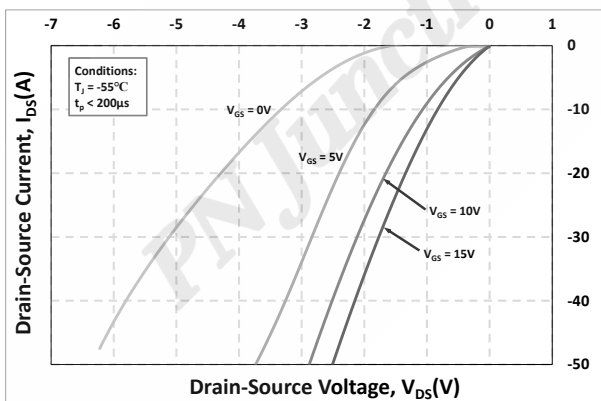


Figure 15. 3rd Quadrant Characteristic at -55°C

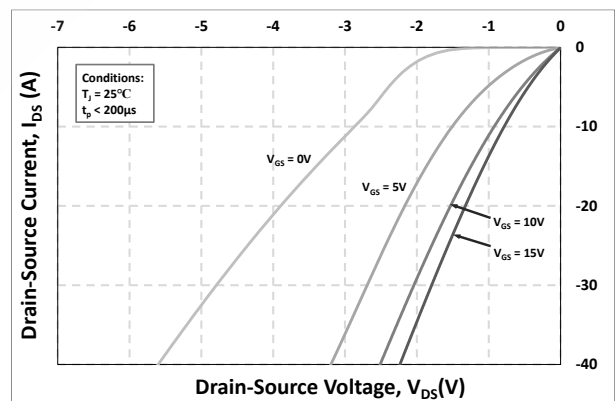


Figure 16. 3rd Quadrant Characteristic at 25°C

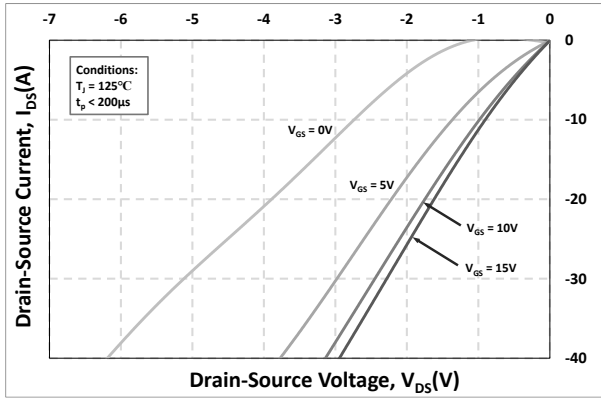


Figure 17. 3rd Quadrant Characteristic at 125°C

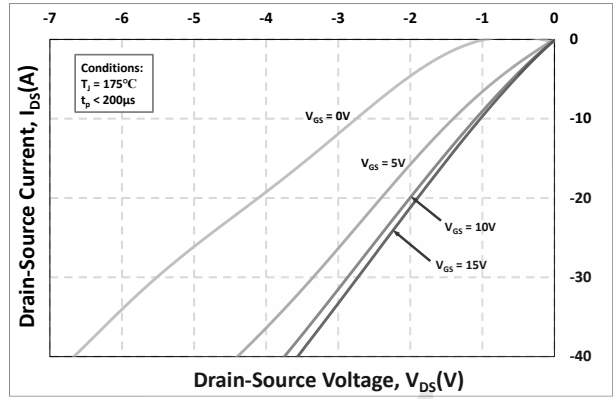


Figure 18. 3rd Quadrant Characteristic at 175°C

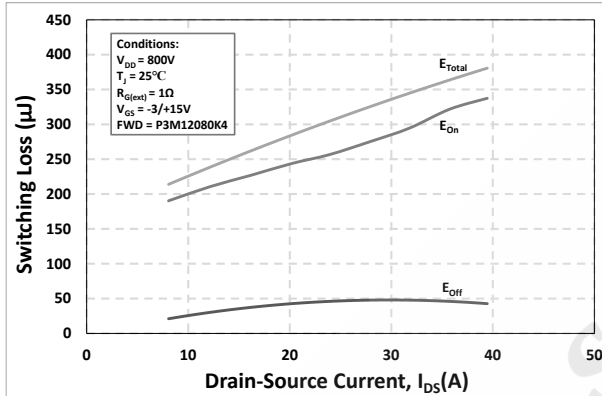


Figure 19. Clamped Inductive Switching Energy vs. Drain Current (VDD= 400V)

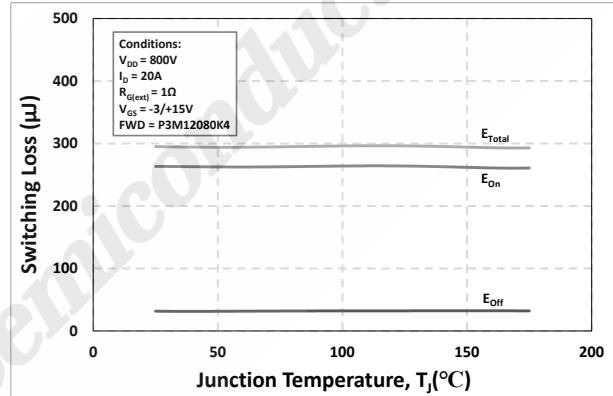


Figure 20. Clamped Inductive Switching Energy vs. RG(ext)

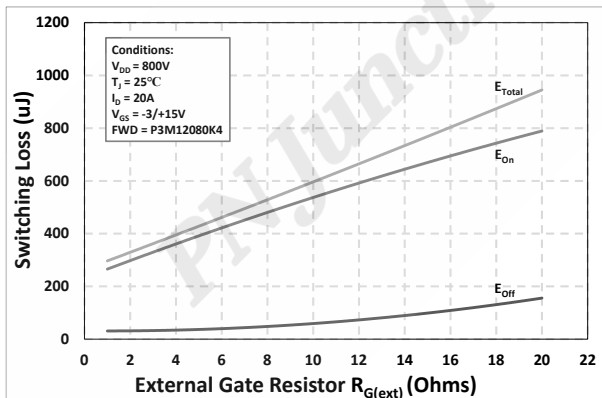


Figure 21. Clamped Inductive Switching Energy vs. Temperature

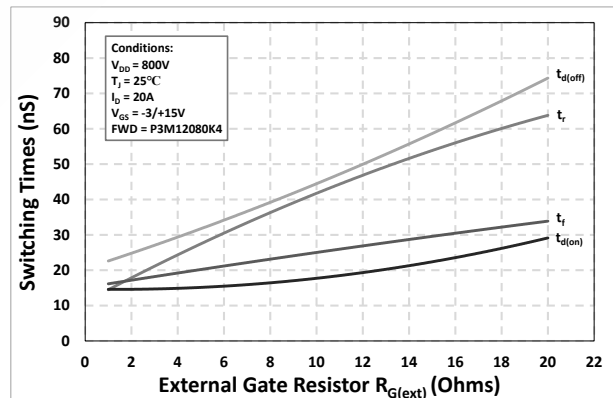


Figure 22. Switching Times vs. RG(ext)

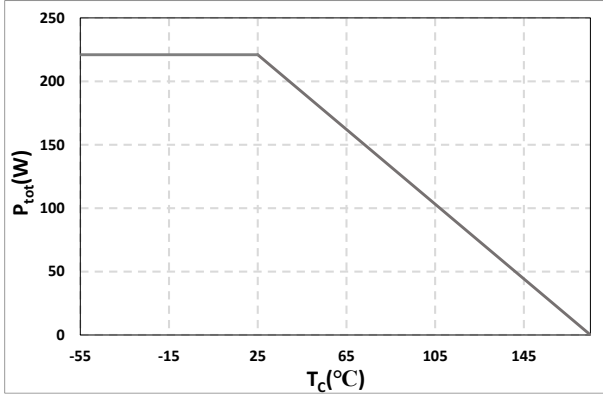


Figure 23. Maximum Power Dissipation Derating vs. Case Temperature

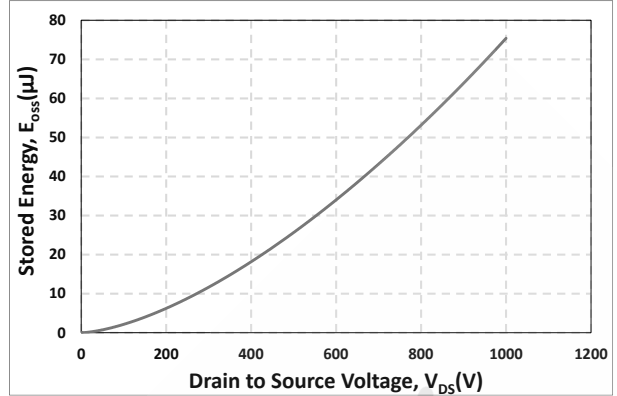


Figure 24. Output Capacitor Stored Energy

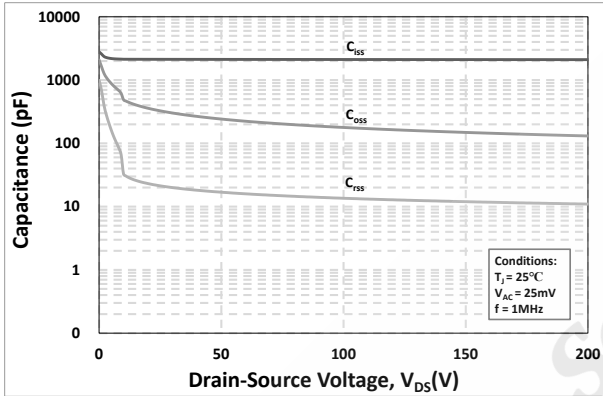


Figure 25. Capacitances vs. Drain-Source Voltage (0 - 200V)

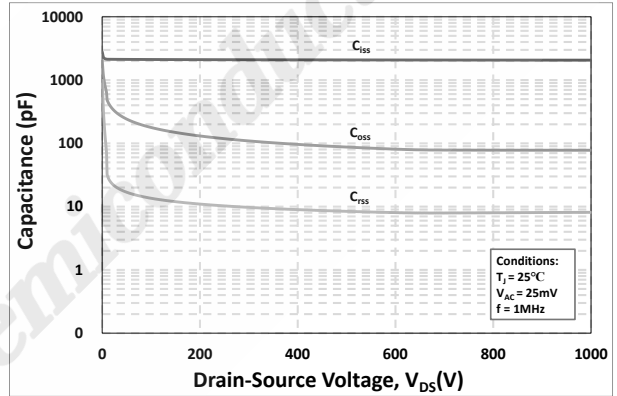


Figure 26. Capacitances vs. Drain-Source Voltage (0 - 1000V)

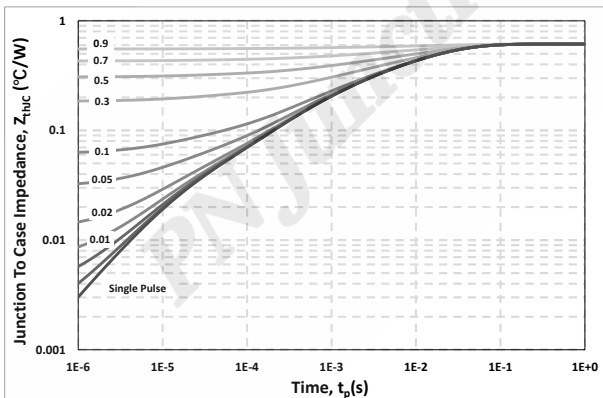


Figure 27. Transient Thermal Impedance (Junction - Case)

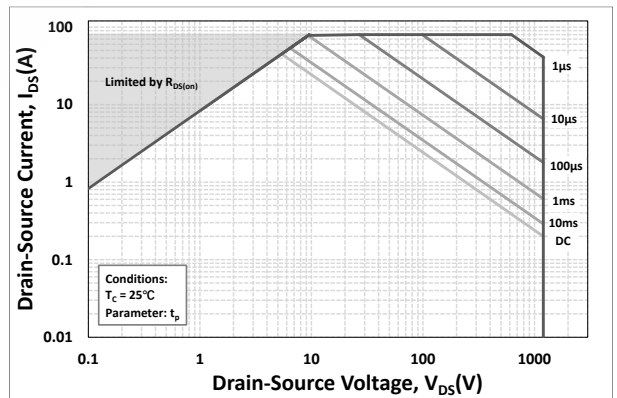
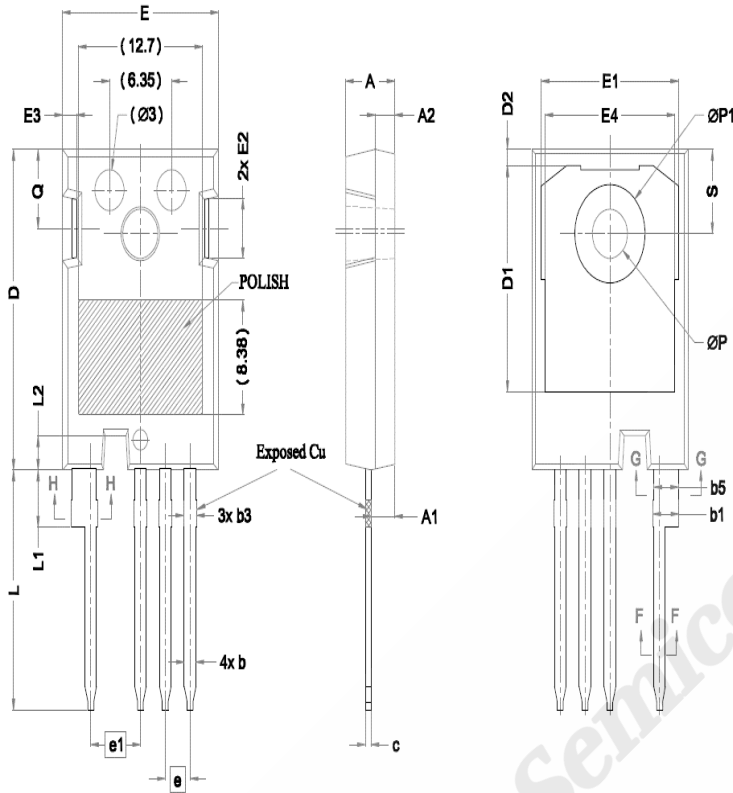


Figure 28. Safe Operating Area

6. Package Outlines



Symbol	Dimensions		
	Min.	Nom.	Max.
A	4.83	5.02	5.21
A1	2.28	2.41	2.54
A2	1.91	2.00	2.16
b ¹	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b2	2.39	2.67	2.84
b3	1.07	1.30	1.60
b4	1.07	1.30	1.50
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	22.30	23.45	23.80
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.60	1.10	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54BSC		
e1	5.08BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
φP	3.51	3.61	3.65
φP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

Drawing and dimensions

PN Junction Semiconductor